# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

# HEF4021B
# MSI
## 8-bit static shift register

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

# 8-bit static shift register

# HEF4021B
# MSI

## DESCRIPTION

The HEF4021B is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input ($D_S$), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs ($P_0$ to $P_7$) and buffered parallel outputs from the last three stages ($0_5$ to $O_7$).

Each register stage is a D-type master-slave flip-flop with a set direct/clear direct input. Information on $P_0$ to $P_7$ is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on $D_S$ is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

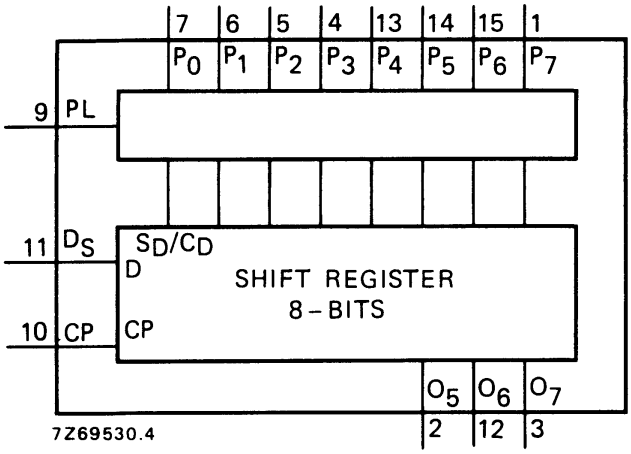


Fig.1 Functional diagram.

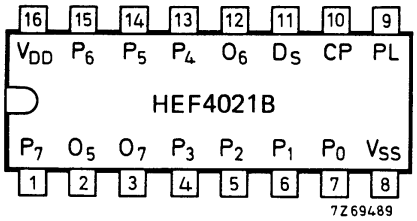


Fig.2 Pinning diagram.

HEF4021BP(N): 16-lead DIL; plastic (SOT38-1)

HEF4021BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF4021BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

**FAMILY DATA, $I_{DD}$ LIMITS category MSI**

See Family Specifications

## PINNING

| | |
|---|---|
| PL | parallel load input |
| $P_0$ to $P_7$ | parallel data inputs |
| $D_S$ | serial data input |
| CP | clock input (LOW to HIGH edge-triggered) |
| $O_5$ to $O_7$ | buffered parallel outputs from the last three stages |

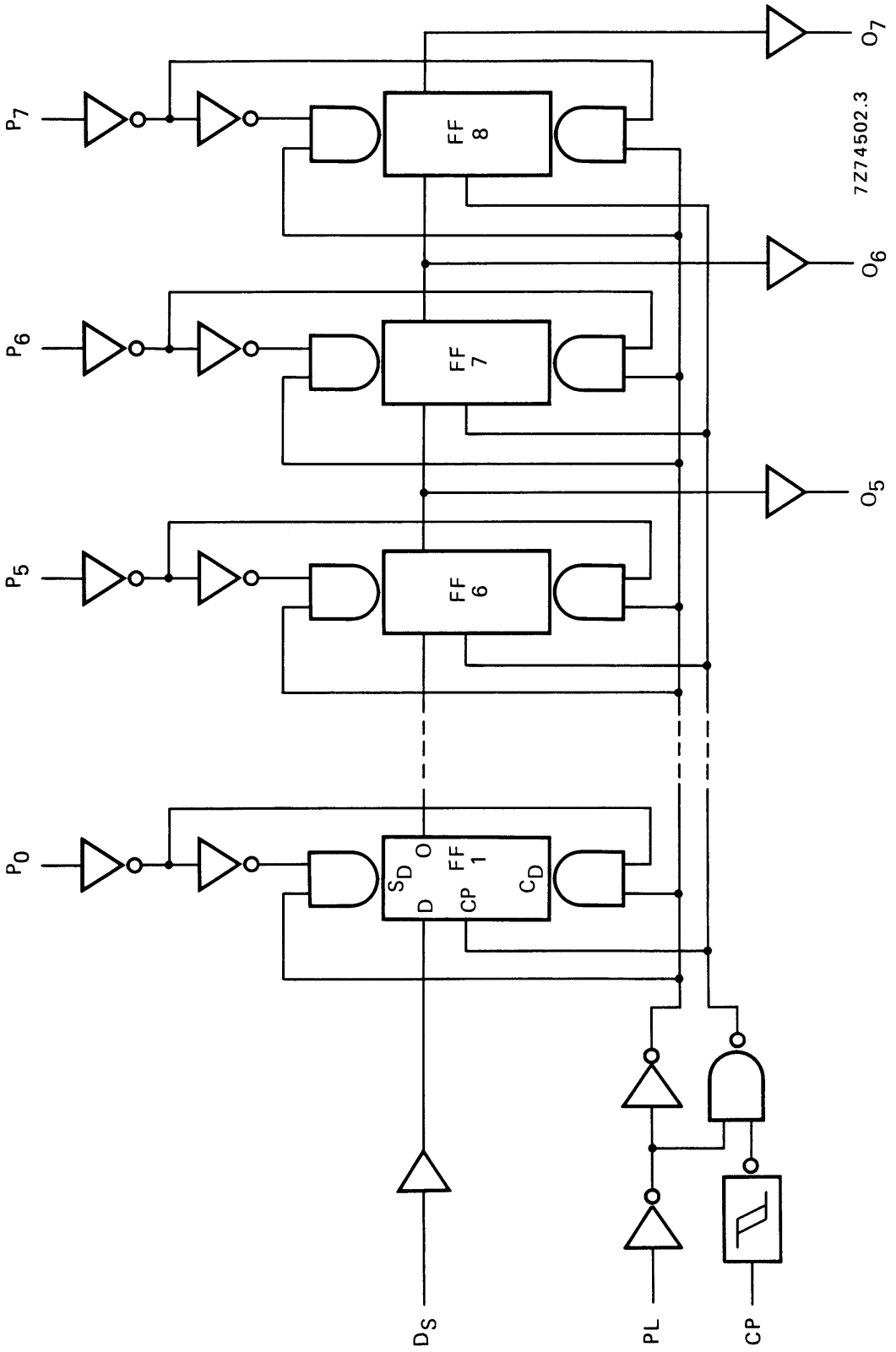


Fig.3 Logic diagram.

## FUNCTION TABLES

Serial operation

| | INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| n | CP | $D_S$ | PL | $O_5$ | $O_6$ | $O_7$ |
| 1 | ↗ | $D_1$ | L | X | X | X |
| 2 | ↗ | $D_2$ | L | X | X | X |
| 3 | ↗ | $D_3$ | L | X | X | X |
| 6 | ↗ | X | L | $D_1$ | X | X |
| 7 | ↗ | X | L | $D_2$ | $D_1$ | X |
| 8 | ↗ | X | L | $D_3$ | $D_2$ | $D_1$ |
| | ↘ | X | L | no change | | |

Parallel operation

| | INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|
| n | CP | $D_S$ | PL | $O_5$ | $O_6$ | $O_7$ |
| | X | X | H | $P_5$ | $P_6$ | $P_7$ |

**Notes**

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   ↗ = positive-going transition
   ↘ = negative-going transition
   $D_n$ = either HIGH or LOW
   n = number of clock pulse transitions

## AC CHARACTERISTICS

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ≤ 20 ns

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | | TYPICAL EXTRAPOLATION FORMULA |
|---|---|---|---|---|---|---|---|
| Propagation delays | | | | | | | |
| CP → $O_n$ | 5 | | | 125 | 250 | ns | 98 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 115 | 230 | ns | 88 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| PL → $O_n$ | 5 | | | 120 | 240 | ns | 93 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 105 | 210 | ns | 78 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 50 | 100 | ns | 39 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| Output transition | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| times | 10 | $t_{THL}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| HIGH to LOW | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |

**AC CHARACTERISTICS**

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ≤ 20 ns

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | |
|---|---|---|---|---|---|---|
| Set-up time | 5 | | 25 | –15 | ns | see also waveforms Figs 4 and 5 |
| $D_S \rightarrow CP$ | 10 | $t_{su}$ | 25 | –10 | ns | |
| | 15 | | 15 | –5 | ns | |
| | 5 | | 50 | 25 | ns | |
| $P_n \rightarrow PL$ | 10 | $t_{su}$ | 30 | 10 | ns | |
| | 15 | | 20 | 5 | ns | |
| Hold times | 5 | | 40 | 20 | ns | |
| $D_S \rightarrow CP$ | 10 | $t_{hold}$ | 20 | 10 | ns | |
| | 15 | | 15 | 8 | ns | |
| | 5 | | 15 | –10 | ns | |
| $P_n \rightarrow PL$ | 10 | $t_{hold}$ | 15 | 0 | ns | |
| | 15 | | 15 | 0 | ns | |
| Minimum clock | 5 | | 70 | 35 | ns | |
| pulse width; LOW | 10 | $t_{WCPL}$ | 30 | 15 | ns | |
| | 15 | | 24 | 12 | ns | |
| Minimum PL | 5 | | 70 | 35 | ns | |
| pulse width; HIGH | 10 | $t_{WPLH}$ | 30 | 15 | ns | |
| | 15 | | 24 | 12 | ns | |
| Recovery time | 5 | | 50 | 10 | ns | |
| for PL | 10 | $t_{RPL}$ | 40 | 5 | ns | |
| | 15 | | 35 | 5 | ns | |
| Maximum clock | 5 | | 6 | 13 | MHz | |
| pulse frequency | 10 | $f_{max}$ | 15 | 30 | MHz | |
| | 15 | | 20 | 40 | MHz | |

| | $V_{DD}$ V | TYPICAL FORMULA FOR P (μW) | |
|---|---|---|---|
| Dynamic power | 5 | $900\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | where |
| dissipation per | 10 | $4\ 300\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_i$ = input freq. (MHz) |
| package (P) | 15 | $12\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_o$ = output freq. (MHz) |
| | | | $C_L$ = load capacitance (pF) |
| | | | $\sum (f_o C_L)$ = sum of outputs |
| | | | $V_{DD}$ = supply voltage (V) |

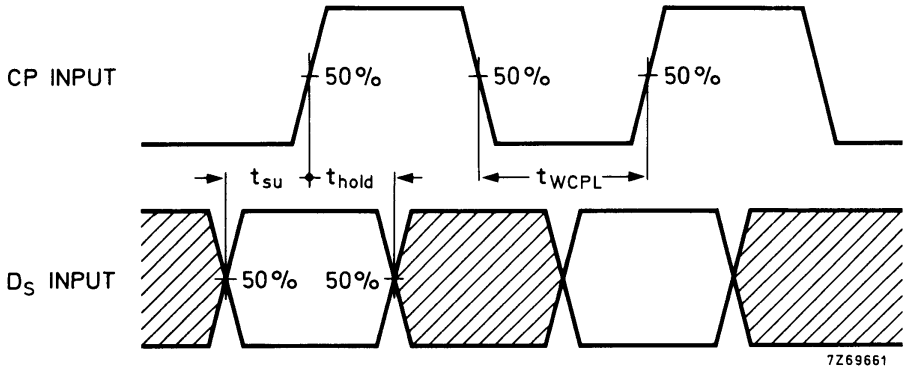


Fig.4 Waveforms showing minimum clock pulse width, set-up time and hold time for CP and $D_S$.

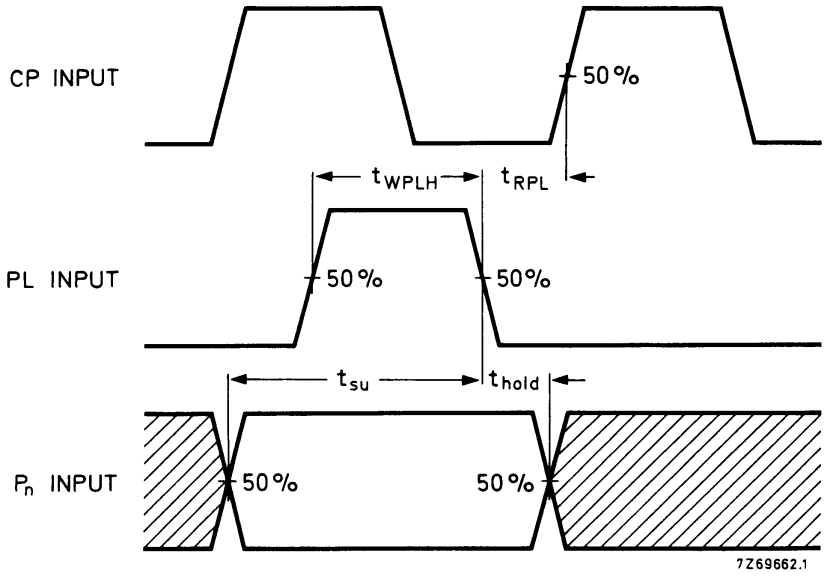


Fig.5 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for $P_n$ to PL. Set-up and hold times are shown as positive values but may be specified as negative values.